Nonlinear Analysis of GaAs MESFET Amplifiers, Mixers, and Distributed Amplifiers Using the Harmonic Balance Technique

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Abstract—**The harmonic balance technique with Newton's method is used to analyze several forms of large-signal operation of GaAs MESFET's, including, for the first time, a multiple-device configuration. Computer programs for the study of the MESFET mixer, intermodulation distortion in MESFET amplifiers, and the large-signal analysis of the MESFET distributed amplifier are described and examples of analyses are given. Convergence properties are excellent, even for cases with a large number of error functions. The choice of time period for analysis, the number of sampling points required, and factors critical to convergence are discussed. Time sampling at much larger than the Nyquist rate does not significantly improve the accuracy and greatly increases the program's execution time.**

I. Introduction

THE "HARMONIC BALANCE" technique [1] has previously been used to develop an accurate analysis of large-signal operation of the GaAs MESFET amplifier [2]. Experimental verification of the accuracy was demonstrated [2]. Kundert and Sangiovanni-Vincentelli [3] described the many advantages of circuit simulators using the harmonic balance technique as compared with time-domain simulation with SPICE [4]. Because of the computational efficiency of the harmonic balance technique and its adaptability to network design problems, the analysis of FET mixers, of intermodulation distortion in FET amplifiers, and of the distributed amplifier was attempted using the same technique. Computer programs for these analyses were successfully developed and are described herein.

II. Harmonic Balance

The GaAs FET model used is the same as that described earlier by Curtice and Ettenberg [2] and is shown in Fig. 1. Model details can be obtained from the reference. However, the analysis technique can be applied to other circuit models for the FET. It is only necessary to determine that the convergence properties have not been adversely affected.

Fig. 2 shows the FET model in a common-source configuration (including source inductance) and shows the notation used for analysis. The voltages to be determined by the harmonic balance method are V_i, the input circuit voltage and V_o, the output circuit voltage. These internal node voltages are used because both gate and drain resistors (R_g and R_d) are absorbed into the linear networks connected to these terminals when analysis is performed. This is part of the partitioning process whereby the circuit is separated into linear and nonlinear parts.

The source voltage V_s presents a special problem. One choice is to include the voltage as an unknown to be determined by the harmonic balance procedure. This is not usually desirable since it increases the number of error functions needed directly as the number of unknown voltages is increased. For all single-device analyses, convergence properties are excellent when V_s is obtained (in the frequency domain) by calculating the source impedance times the current flow. In the case of the distributed amplifier, updating the source voltage value each iteration of the harmonic balance procedure produces divergence. A simpler procedure was used instead and checked with the more accurate approach of including V_s in the harmonic balance procedure.

Each unknown voltage has a real and an imaginary part. Assuming fundamental and second-harmonic voltage, each voltage has four amplitudes associated with it and, therefore, four error functions to be minimized to produce a self-consistent solution. Omitting V_s, there are then eight amplitudes and eight error functions associated with each FET. If third-harmonic voltages are included, then there are 12 amplitude and error functions per FET.

The harmonic balance (HB) technique consists of an iteration procedure to find a steady-state solution for all voltage amplitudes. These voltage amplitudes produce current into the linear circuit that is the same as the current into the connecting nonlinear circuit within some small error. For a valid solution, the RMS sum of all (current) errors must be less than a small number chosen by the user. The factor ERRMAX is defined as the ratio of the RMS current error to the dc drain–source current. For this study, ERRMAX is between 10^{-4} and 10^{-6}.

The HB technique for the amplifier consists of a time-domain model of the GaAs MESFET coupled with frequency-domain models for the input- and output-

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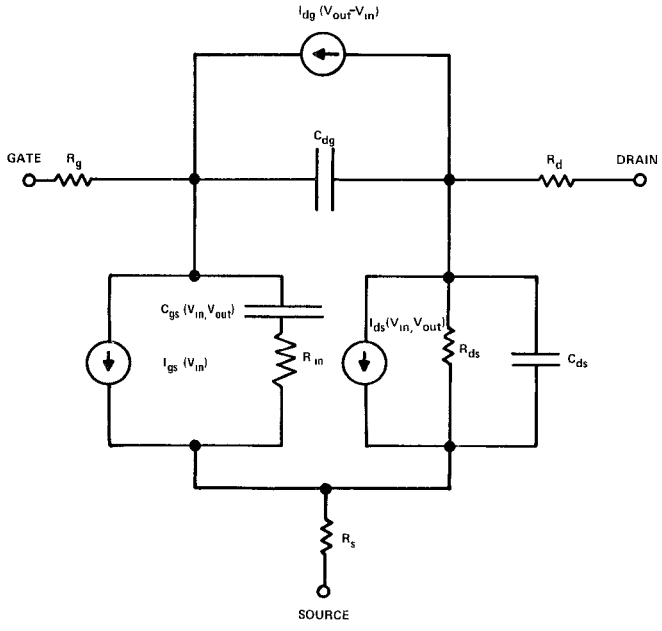

Fig. 1. Large-signal equivalent circuit model for the GaAs MESFET.

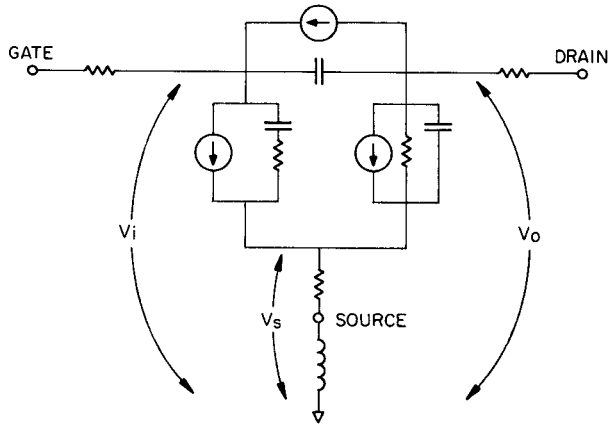

Fig. 2. Voltage notation for the FET.

matching circuits. The nonlinear FET elements must be analyzed in the time domain to most accurately simulate the actual device. The linear circuit response to the FET current excitation can be analyzed in the frequency domain by standard techniques. Transformation between the time and the frequency domain is accomplished using a discrete Fourier transform. A valid physical solution is obtained when the voltage waveform at the input (or output) of the FET produces a current waveform into the device that is the negative of that into the RF circuit to within some small error. The program flow chart is shown in Fig. 3.

The HB technique has been described in detail by Kundert and Sangiovanni-Vincentelli [3]. The iterative procedure used here is a modification of their equation (18) for Newton's method. An update factor, α, has been added:

$$v^{(j+1)} = v^{(j)} - \alpha\left[J_\epsilon(v^{(j)})\right]^{-1}\epsilon(v^{(j)})$$

where $v^{(j)}$ is the jth iteration of the voltage vector con-

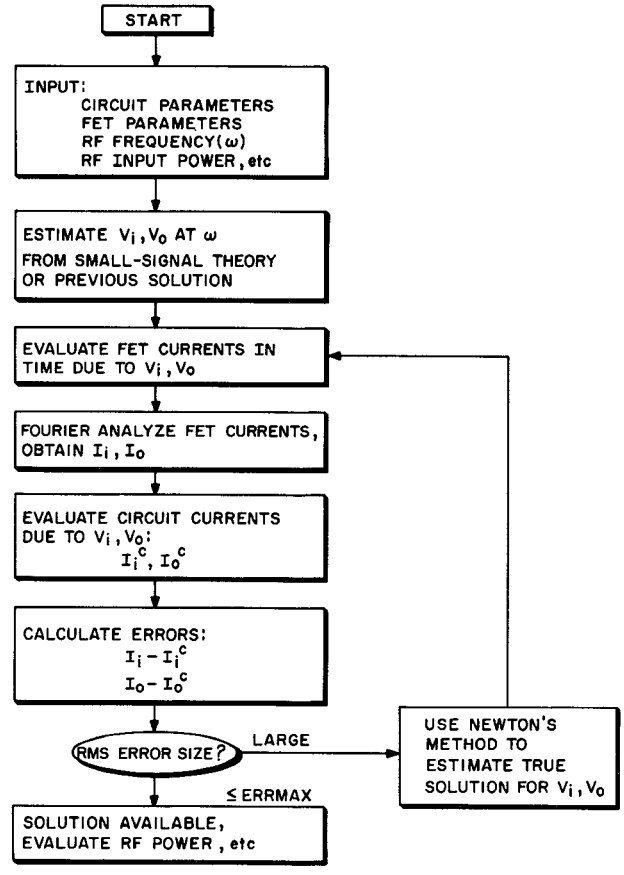

Fig. 3. Flow chart for the analysis of the FET amplifier using the HB technique.

taining the complete voltage spectrum for each node, α is the update coefficient ($0 < \alpha < 1$), $J_\epsilon(v)$ is the complete harmonic Jacobian at v, and $\epsilon(v)$ is the error vector. The Jacobian is evaluated numerically in the present program. This procedure is more general in that it does not require the nonlinear elements to be described by power series expansions.

The addition of the update factor α provides damping and better convergence properties. The number of iterations to convergence is usually found to be minimum near $\alpha = 0.5$ (i.e., 50-percent update).

III. The GaAs FET Mixer

A study was made to see if the HB technique can be used for analysis of GaAs FET mixer operation. The FET device model used is only slightly different from the one used for amplifier analysis; however, the circuit model is quite different. The local oscillator power (P_{LO}) and signal power (P_{SIG}) are supplied to the gate at frequency f_{LO} and f_{SIG}, respectively. Typically, $P_{LO} \gg P_{SIG}$. Only the IF voltage is assumed to exist in the drain circuit, because a low-pass filter is used in the actual circuit. A low-pass filter presents very low impedance to higher frequency signals. The IF frequency is either

$$f_{SIG} - f_{LO}$$

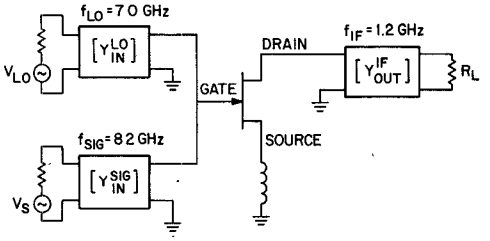

Fig. 4. FET mixer circuit.

TABLE I
LO, SIG, AND IF POWERS AND THE ERROR AS A FUNCTION OF ITERATION NUMBER IN THE HB SOLUTION OF A GaAs FET MIXER

Iteration	Input LO Power	Input SIG Power	Output IF Power	RMS Error
0	0.0000E +00	0.0000E +00	0.0000E +00	0.0000E +00
1	-0.8394E -02	0.5084E -04	0.5866E -03	0.2446E -02
2	0.5078E +00	0.8029E -02	0.1568E +00	0.2045E -02
3	0.6095E +00	0.9108E -02	0.1237E +00	0.1013E -02
4	0.6239E +00	0.8406E -02	0.7788E -01	0.4945E -03
5	0.6221E +00	0.7994E -02	0.5786E -01	0.2435E -03
6	0.6189E +00	0.7898E -02	0.5078E -01	0.1196E -03
7	0.6169E +00	0.7870E -02	0.4792E -01	0.6018E -04
8	0.6158E +00	0.7853E -02	0.4648E -01	0.3006E -04
9	0.6152E +00	0.7850E -02	0.4586E -01	0.1516E -04
10	0.6149E +00	0.7847E -02	0.4552E -01	0.7631E -05
11	0.6147E +00	0.7846E -02	0.4537E -01	0.3854E -05

or

$$f_{LO} - f_{SIG}.$$

Either case will work with little difference in the results.

The example being analyzed is described by Maas [5] and is shown in Fig. 4. In this example, the LO frequency is 7.0 GHz, the SIG frequency is 8.2 GHz, and the IF frequency is 1.2 GHz.

All frequencies are harmonics of a lower frequency f_0. For this case, the IF, LO, and SIG frequencies are 6th, 35th, and 41st harmonics of the frequency $f_0 = 200$ MHz. One period of the frequency f_0 must be used to find the current waveform of the FET. This is sufficient since a valid solution over one period of f_0 will repeat identically the next cycle. The number of time samples taken during this period need only be equal to or greater than the Nyquist rate. This is approximately twice the highest harmonic number. Tests with five times this number did not increase the accuracy and greatly increased the execution time.

Table I shows a typical solution for the FET mixer using the new analysis program. The first column is the iteration number. The powers are then listed in mW. The last column is the RMS (current) error. A 50-percent update is used in each iteration and this produces monotonic convergence (as seen by inspection of the error column). The final solution shows that an IF output of 45.37 μW results from a signal input of 7.846 μW with an LO power of 0.6147 mW.

Fig. 5 shows the large-signal equivalent circuit model for the GaAs FET and the voltage notation. The linear circuit elements corresponding to gate and drain resistance and inductance are included in the two-port networks.

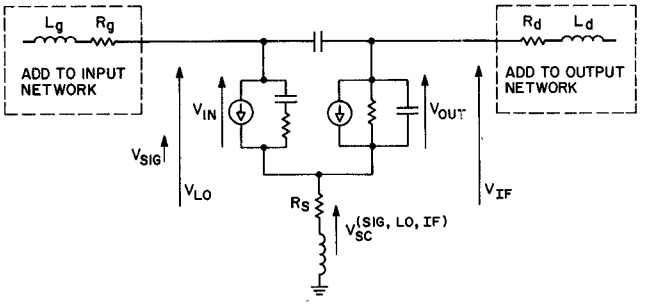

Fig. 5. FET equivalent circuit and voltage notation for the mixer.

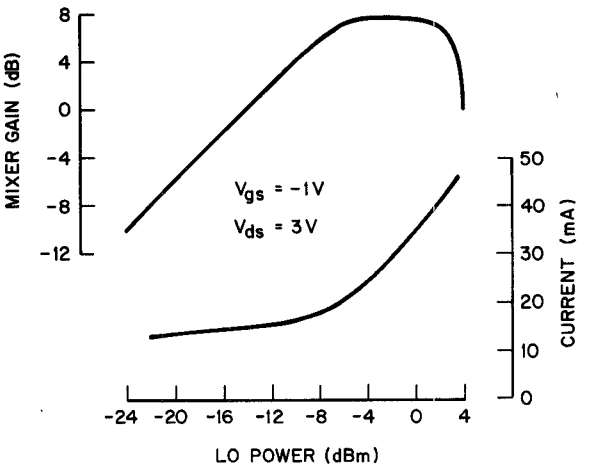

Fig. 6. Mixer gain and FET dc drain current as a function of LO power.

Drain–gate breakdown current is omitted in Fig. 5 as it will not occur. The drain voltage changes very little from the dc bias value since no LO power exists in the drain circuit.

The FET model uses the transistor parameters measured by Maas. Unfortunately, Maas has only presented current–voltage (I–V) data and capacitance data for the device. No RF data are available. Without any RF evaluation (such as S-parameter data), the FET is not sufficiently characterized and the equivalent circuit element values have large uncertainty. For analysis, unknown transistor circuit element values were estimated from RCA devices.

The input circuits for LO and SIG were designed for near matches to 50-Ω sources. An output IF load of 70 Ω was used, as in the experimental tests.

Fig. 6 shows the computed mixer gain (i.e., P_{IF}/P_{SIG}) and bias current as a function of LO power. Notice the gain dependence upon LO power; this is similar in behavior to that measured by Maas. Notice the current dependence upon LO power at large LO power.

Fig. 7 shows the effect of gate bias changes. The mixer's gain is largest at approximately −1.1 V. This effect is dependent upon the nonlinearity of the device. It is useful to evaluate the circuit elements of the FET that have the largest effect upon the mixer gain. Study showed these elements to be (1) the nonlinearity in transconductance and (2) drain–source conductance.

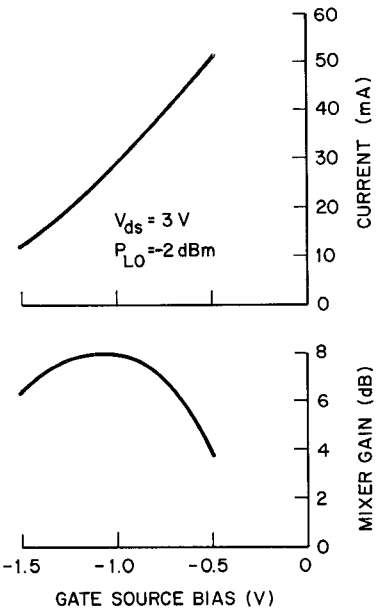

Fig. 7. Mixer gain and FET dc drain current as a function of gate–source bias voltage.

IV. FET Amplifier Intermodulation Distortion

The evaluation of third-order intermodulation distortion (IMD) in FET amplifiers has been accomplished using the HB method of analysis. A single-stage GaAs FET amplifier was analyzed with a computer program developed to accommodate multiple input and output signals. Time-domain samples are taken at the Nyquist rate, rather than a reduced rate, as Gilmore and Rosenbaum [6] have done. Execution time is reduced by other means.

Fig. 8 shows the circuit used for the IMD analysis. Two input signals are used at frequencies f_1 and f_2. The input circuit is assumed identical for each signal since the signal separation is small (about 10 MHz). The output network is optimized for large-signal operation and four signals are present: f_1, f_2 and the intermodulation signals $f_3 = 2f_1 - f_2$ and $f_4 = 2f_2 - f_1$.

All four frequencies are taken to be harmonics of a fundamental low frequency f_0. Let

$$N = f_2/f_0$$

where N is large, at least 100. It is not necessary to make f_0 equal to the actual difference frequency $f_2 - f_1$, i.e., $N = f_2/(f_2 - f_1)$, because little change occurs for large values of N.

During development, it was observed that much computational time was occupied computing Fourier coefficients of number 1 to $2N$. In fact, the only coefficients required are $N-2$, $N-1$, N, and $N+1$, corresponding to the frequencies f_3, f_1, f_2, and f_4, and $2N-2$, $2N$, corresponding to $2f_1$ and $2f_2$. By omitting the computation of all except these six, the program's execution time was reduced by a factor of 10 to a typical execution time of 8 min on a VAX 11/780 with a floating-point accelerator.

Each signal is complex, having real and imaginary parts. An error function must be defined for each part. Since f_1 and f_2 are at the input and output and have harmonics, there are eight error functions associated with each signal. Signals f_3 and f_4 exist at input and output but their harmonics are neglected since they are weak. There are then only four error functions associated with each of these signals. There are then 24 amplitudes (and error functions) to be determined at each operating condition. It is interesting that the HB technique works well in this situation. For 50-percent update in each iteration, convergence is monotonic and rapid.

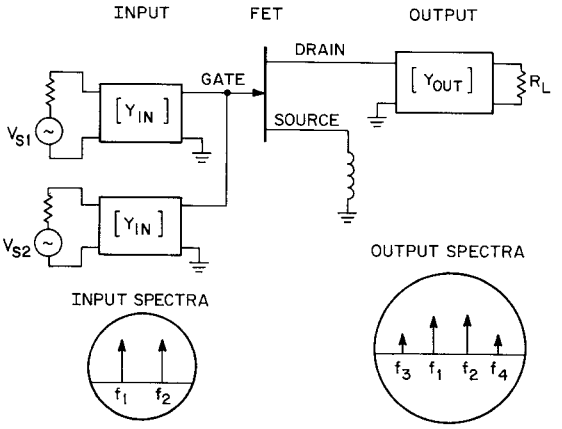

Fig. 8. Circuit for FET amplifier IMD tests.

TABLE II
IMD Program Results for Two-Tone Test of FET B1512-3A

Time Divisions (No.)	f_1 Output Power (mW)	f_1 Input Power (mW)	IMD Signals Lower (mW)	IMD Signals Upper (mW)
405	98.24	20.82	1.2129	1.2112
500	102.70	20.86	1.2261	0.9241
801	98.46	20.83	1.2189	1.2217

(ERRMAX = 1E-4).

A second important consideration is the choice of the number of time samples in the low-frequency period f_0. The number of time divisions used for analysis was varied to determine if the accuracy was affected. Table II shows the result of the study. The minimum number of time divisions is 405. This occurs due to the Nyquist sampling requirement of the Fourier analysis routine ($N \cong 100$).

The choice of the number of time division is important, since a poor choice can cause large errors. Table II shows that there is little difference in the f_1 signal amplitudes for 405 (the minimum number) or 801 (approximately twice the minimum number) time divisions. The example of 500 divisions is shown in Table II. This choice causes inaccuracy in the amplitude of the output power at f_1 because it causes many of the sampled amplitudes of frequency f_1 to be redundant. The conclusion from this study is that use of the minimum number of time divisions does not reduce the accuracy and is desirable due to reduced execution time. In addition, the choice of the number of time divisions must be such that it does not include duplicate waveform samples.

Fig. 9 shows the HB IMD program results for a two-tone test of a FET of 600-μm periphery. The two-tone test is

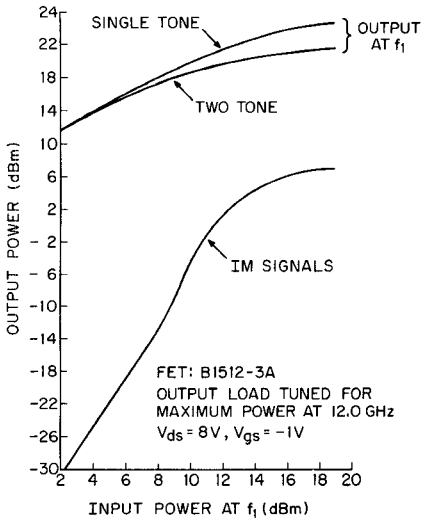

Fig. 9. Calculated output signal powers at f_1 and f_2 and IM frequencies ($2f_1 - f_2$, $2f_2 - f_1$) as a function of input power for two-tone tests with equal input power of FET B1512-3A.

TABLE III
EXPERIMENTAL AND THEORETICAL COMPARISON OF IMD FOR FET B1512-3A AT 12 GHz

	2-Tone Power Output (dBm)	IMD Output Lower (dBc)	IMD Output Upper (dBc)
Experimental	11.2	41.0	37.5
Computed	11.5	40.0	40.1

made with equal power at frequencies of f_1 and f_2, both near 12 GHz. The output power at either f_1 or f_2 is seen to be reduced in the two-tone test as compared to single-frequency operation, and the IMD signals are observed. Notice that the IMD signals do not follow a third-power slope at high drive level. In this region, it is expected that the Volterra [7] series approach would be inaccurate.

Experimental verification of the IMD program was made using a two-tone test with frequency separation of 5 MHz at 12 GHz for FET No. B1512-3A. The amplifier was tuned for maximum small-signal gain, and the data are shown in Table III. The IMD computed is within a few dB of the measurement, which is about the same as the measurement error. A recent experimental study for a wide range of load conditions and drive powers also showed good agreement with IMD calculations. These data will be available for publication in the near future.

V. THE DISTRIBUTED AMPLIFIER

A particular multiple-FET circuit of great importance is the FET distributed amplifier. We have successfully investigated the large-signal analysis of a distributed amplifier using the HB technique and will show analysis of a four-stage amplifier similar to that described by Ayasli *et al.* [8].

Fig. 10 shows the circuit assumed for the four-stage amplifier. It consists of an input five-port network with Y-parameters $[Y_i]$, an output five-port network with Y-parameters $[Y]$, and four FET devices. Each FET is modeled as shown in Fig. 11. The voltage notation in the frequency domain for the Lth FET is, for fundamental frequency:

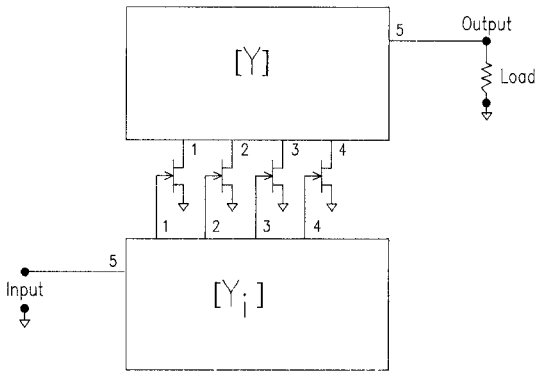

Fig. 10. FET distributed amplifier circuit.

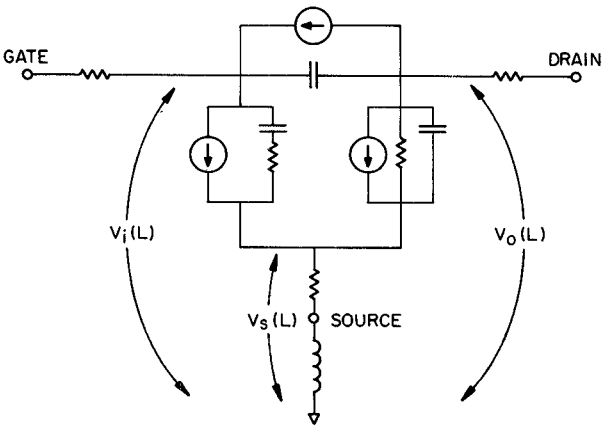

Fig. 11. Voltage notation for each FET in the distributed amplifier.

$$V_i(L) = \text{gate'-to-ground voltage}$$
$$V_o(L) = \text{drain'-to-ground voltage}$$
$$V_s(L) = \text{source'-to-ground voltage.}$$

The primed terminals are the device side of the resistor attached to that terminal. The notation at second harmonic is the same except for the addition of the suffix 2.

The output circuit current at the jth port, I_j, is calculated in the frequency domain as

$$I_j = \sum_{L=1}^{L=5} Y_{jL} \cdot V_o(L).$$

Since the load is 50 Ω,

$$\frac{I_5}{V_o(5)} = -0.02$$

and by using the previous equation, it can be shown that

$$V_o(5) = \frac{-\sum_{L=1}^{L=4} Y_{5L} V_o(L)}{Y_{55} + 0.02}.$$

Therefore, in the HB procedure, once values of $V_o(1) \cdots$

$V_o(4)$ are chosen, $V_o(5)$ is known and the current at any port (I_j) can be evaluated. The expression for $V_i(5)$ is slightly different due to the presence of the voltage source but was found in the same manner. For second-harmonic voltages, the input and output networks are assumed to be four-port networks with a 50-Ω load at the port previously designated as the fifth port.

Both $V_i(L)$ and $V_o(L)$ have real and imaginary parts, as do the second-harmonic voltages. Thus, there are eight unknown voltages per FET and eight error functions per FET. The source voltage $V_s(L)$ and its second harmonic $V_{s2}(L)$ are found from a small-signal estimate that is later updated to a value obtained when the error function is low. This value is equal to the RF current times the source impedance (including source inductance). This results in about 5-percent error in each source voltage. We must determine if this inaccuracy is a problem. Tests to be described show that small source-voltage errors do not significantly affect results.

Several other methods for evaluating source voltages were tried and all produced poor results, namely, divergence rather than convergence. This includes the method of updating the source voltage each cycle, but using only 0.1 percent of the new value and 99.9 percent of the old value. The source voltage produces strong feedback and can cause numerical instabilities.

Thirty-two error functions are utilized in the four-FET distributed amplifier. In spite of this large number, convergence is monotonic for all cases we have analyzed.

We initially thought that it would be necessary to estimate all the fundamental-frequency voltage amplitudes from small-signal analysis to start the iteration procedure. We have found that arbitrary initial guesses are very nearly as good. The present program assigns 1 V to each fundamental voltage and 0.01 V to each harmonic voltage regardless of the actual input power. This procedure has worked in all the cases we have analyzed. If one desires a set of solutions, each with successively larger input power, it generally is faster to use each previous solution as an initial guess for the new solution.

The amplifier simulated is a MMIC design being developed at RCA Laboratories. The input and output networks are transmission lines that have been optimized for operation between 8 GHz and 17 GHz. We chose to operate it at 11 GHz. The small-signal insertion gain calculated by SUPER-COMPACT™ [9] is 8.4 dB. Our HB analysis predicts 8.2 dB gain, which is good agreement. Table IV shows the power saturation characteristics calculated at 11 GHz using the HB program.

The execution time for the initial case of 10-mW incident power is 78 s on the VAX 11/780. The other cases were about 1 min each. The execution time for a SPICE simulation of a similar problem is about 65 min.

A second version of the distributed amplifier program was written. This program treats the source voltages as unknown voltages to be determined during the HB process. The disadvantage of this procedure is that 12 error functions are required per FET compared to eight per FET for the previous program. For the four-FET distributed amplifier, there are then 48 total error functions that must be minimized simultaneously. We believe such a program would be a good test for the HB procedure and would serve as a better solution with which the earlier program may be compared.

TABLE IV
POWER SATURATION CHARACTERISTICS CALCULATED BY THE HB PROGRAM FOR FOUR-STAGE DISTRIBUTED AMPLIFIER

Input Power (mW)	Output Power (mW)	Gain (dB)
9.85	64.76	8.2
39.5	224.9	7.6
61.9	299.9	6.9
89.2	353.5	6.0
120.9	392.6	5.1
156.7	422.5	4.3

(ERRMAX = 2.E-5).

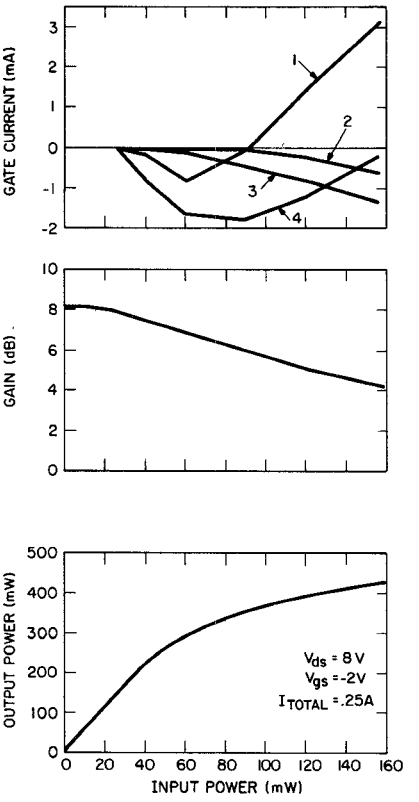

Fig. 12. Direct-current gate currents for devices 1–4, gain and output power for the MMIC distributed amplifier as a function of input power.

The new program is successful and does converge. The execution time is increased by 40 percent but the convergence properties are very similar. The output power calculated by two programs differs by less than 1 percent in all cases. These results prove that the earlier program is sufficiently accurate for power calculations.

Fig. 12 shows graphs of the power saturation characteristics, gain, and dc gate current calculated for the MMIC amplifier chip. The results illustrate how the program can help diagnose problems in the MMIC chip and thus be an invaluable aid for the MMIC designer.

The lower curves in Fig. 12 show output power and gain as a function of input power. The linear circuit design was

optimized using SUPER-COMPACT and does not perform well at high input power when saturation occurs. The HB program allows the designer to change the linear circuit and see the effects in the saturation characteristic.

The top curves in Fig. 12 show the gate current at each device. All devices go into avalanche breakdown as input power is increased, as indicated by negative gate current. Device number one becomes forward biased at larger input power, as indicated by positive gate current. If such a MMIC chip burns out as drive power is increased up to 100 mW, the problem is with device number four, as it has the largest breakdown current. If burnout occurs at 150 mW input power, the problem is the excessive forward biasing of device number one.

All other aspects of the individual operation of the MESFET's may be studied using this program. The use of the program as a design tool should then permit the MMIC designer to achieve optimum results with fewer experimental test vehicles.

VI. Conclusions

Programs for the analysis of the GaAs MESFET mixer, of IMD in GaAs amplifier, and of the GaAs distributed amplifier have been successfully developed. The harmonic balance technique was used with a damped Newton method and convergence properties were found to be excellent, even for a case with 48 error functions. These results illustrate how powerful the harmonic balance technique is and how it may be utilized in nonlinear circuit designs. The harmonic balance technique should provide the basis for the development of a new family of CAD design tools that will provide optimization and tolerancing for nonlinear circuits.

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